

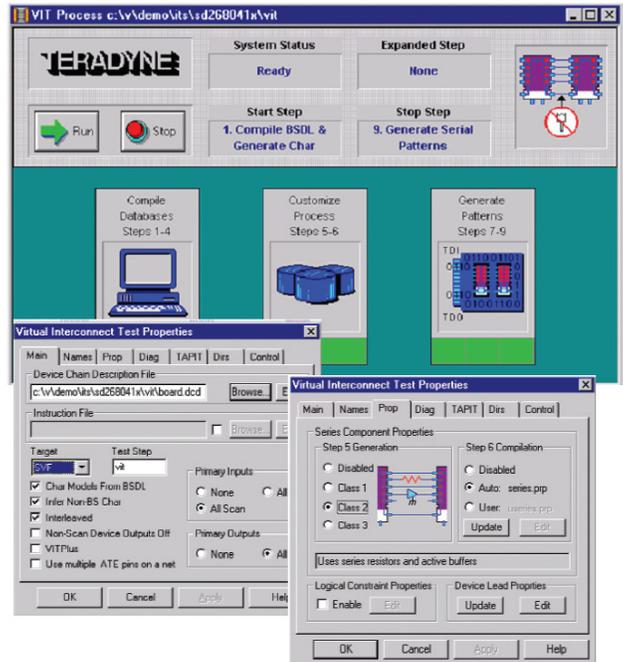
VICTORY Boundary-Scan Software

Comprehensive Capabilities for Generating Tests and Diagnostics

Teradyne's VICTORY™ software is a comprehensive toolset for test generation, program development, and diagnostics for boards designed with boundary-scan devices. VICTORY allows test developers to take full advantage of the greater access that boundary-scan provides. It is capable of greatly simplifying testing and improving fault coverage in cases where physical access for test is limited.

FEATURES

- *Complies fully with IEEE Std 1149.1 and BSDL industry standards*
- *Verifies the integrity of BSDL models and TAP connections*
- *Automatically generates test patterns for in-circuit and interconnect test of boundary-scan devices*
- *Serializes standard component or cluster patterns to test non-scan nets via the scan path*
- *Supports internal device test techniques: INTEST, BIST, and internal scan*
- *Performs access analysis to optimize test point placement*
- *Ensures transportability to any test environment using standard Serial Vector Format (SVF)*
- *Generates high resolution diagnostics to run on a wide selection of ATE or offline repair stations*
- *Process-oriented GUI simplifies boundary-scan test development and helps get new users productive quickly*



Most assemblies manufactured these days typically have a mix of scan and conventional technologies, and it is rare to come across a “pure” boundary-scan assembly. But, whatever the ratio of scan to non-scan components, VICTORY can use any boundary-scan logic available—even a single 1149.1 device—to simplify test generation and add valuable access points for observation and control.

The complete VICTORY software toolset consists of five test generation modules, plus a fault diagnostic module that is installed on your test system:

- Boundary In-Circuit Test (BICT)
- Virtual Interconnect Test (VIT)
- Virtual Component / Cluster Test (VCCT)
- Boundary Functional Test (BFT)
- Access Analyzer (AA)
- Boundary-Scan Intelligent Diagnostics (BSID)

These test generation modules give you the freedom to design the right test strategy, based on your test objectives and the degree of access available for test. Access Analyzer's testability tools help designers optimize the location of test points on new designs, and the Boundary-Scan Intelligent Diagnostics (BSID) module isolates test failures fast, identifying the failing device, the fault type, and the nets involved.

VICTORY Test Packages

Because test requirements vary, VICTORY modules are conveniently bundled in packages targeted for specific component and board test applications:

■ Component Test Package -

VICTORY's Component Test Package includes the BICT and BFT modules for detecting failures within boundary scan devices, or on their leads. It is ideal for complimenting an in-circuit test strategy when there are boundary-scan devices on your boards. VICTORYNet, a circuit netlist conversion-tool based on Router Solutions' OMNINET, is included in the package. It is capable of importing dozens of CAE board netlist formats for use with VICTORY.

■ Board Interconnect Test Package -

VICTORY's Board Interconnect Test Package is the perfect solution for developing high fault coverage test on printed circuit assemblies with limited in-circuit access, or for system-level scan test challenges. It consists of the VIT and VCCT modules which provide fault coverage on and between boundary scan devices as well as on non-scan device connected to boundary scan components. The Board Interconnect Test Package also includes VICTORYNet.

■ Virtual Test Package -

The Virtual Test Package includes all five VICTORY test generation modules plus VICTORYNet to address any boundary-scan test problem you may encounter.

VICTORY Test Modules

Boundary In-Circuit Test (BICT) Automates Testing of Scan Devices

The BICT module generates test patterns for in-circuit testing of boundary-scan devices. It provides 100% pin-level fault coverage for opens and stuck-at faults where there is full bed-of-nails access to the signal pins of the device-under-test. It is the only VICTORY module that requires physical access to boundary-scan device pins.

BICT generates patterns automatically from the BSDL model of a boundary-scan device. Patterns are stored in a standard test library, together with conventional in-circuit device patterns. A tester uses both conventional and BICT patterns to create a complete in-circuit test program.

BICT includes the following capabilities:

- Automatic verification of a BSDL model's description of the device's 1149.1 circuitry.
- 100% pin-level fault coverage for open/stuck-at faults on scan devices with bed-of-nails access.
- Automatic control of the scan chain during conventional in-circuit testing of non-scan devices.
- Automatic accounting for physical device constraints dictated by board design, such as pins tied to power or ground, pins tied together, and pins with no access.
- Logical device constraints to selectively disable device leads or prevent leads from being tested throughout a BICT test sequence.

Boundary Functional Test (BFT) Finds Faults in Internal Device Logic

The BFT module uses the optional built-in test features available on some boundary-scan devices to test internal device logic as part of an assembly or board-level test.

BFT is an effective toolset for manufacturers required to retest internal device logic as part of the assembly process and for repair depots responsible for isolating failures in the field.

BFT supports four techniques for internal testing of 1149.1 devices:

- Functional test of the device TAP and scan register circuitry
- Device logic test using the 1149.1 INTEST instruction
- Device logic test using internal scan technology
- Device logic test using the 1149.1 RUNBIST instruction

The BFT module automatically generates patterns for functional test of the TAP. For the three other techniques, BFT reconfigures device-oriented patterns into chain-level test patterns that can be applied through the TAP.

Device-oriented patterns and procedures are supplied by test developers in standard Serial Vector Format (SVF), a boundary-scan vector interchange language developed jointly by Texas Instruments and Teradyne.

For the INTEST instruction, test developers often reuse patterns from in-circuit or simulation pattern libraries and serialize them for input to BFT. Patterns for internal scan devices are typically generated by automatic test pattern generation (ATPG) tools. For built-in self test, which requires very simple pattern generation, it is easy to generate test

patterns directly in SVF format.

Virtual Interconnect Test (VIT) Offers 100% Pin-Level Fault Coverage

The VIT module generates patterns to test boundary-scan nets using only the virtual access provided by the boundary-scan circuitry.

On pure boundary-scan nets, VIT verifies that every device is operational at the pin level and that every interconnect is intact - from silicon to lead bonds, from solder bonds to the circuit board itself. VIT patterns can also verify the interconnections of an assembly's primary inputs and outputs, if tester access is available.

VIT patterns are generated automatically from a circuit netlist and the BSDL models of the boundary-scan devices. VIT testing eliminates complex pattern generation, reduces the number of test pads required for 100% detection of structural faults, and simplifies test hardware requirements.

VIT includes the following capabilities:

- 100% detection of stuck-at pin faults and shorts/opens between boundary-scan devices, including devices with differential lead pairs.
- 100% detection of shorts between boundary-scan nets and non-scan nets where the non-scan nets have bed-of-nails access
- Correct testing of boundary-scan nets connected by series components such as in-line resistors and non-scan buffers, reducing the number of test points and improving fault coverage
- Logical device constraints to selectively disable device leads, or hold nets at a constant state, throughout a VIT test sequence
- Control over the number of nets that switch simultaneously with each scan vector. This is important for reducing the effects of ground bounce during test execution.

Virtual Component/Cluster Test (VCCT) Extends Access to Non-Scan Circuitry

The VCCT module uses boundary-scan access to detect open and stuck-at faults on the leads of non-scan devices, eliminating the need for physical access to the signal pins of those devices. VCCT can be used to test a single non-scan component or a cluster of non-scan components.

VCCT uses the scan cells of boundary-scan devices as virtual ATE channels to drive stimulus into the non-scan logic and detect response. VCCT can also use a combination of virtual channels and real ATE channels for driving and detecting.

Stimulus patterns are conventional, parallel test patterns which VCCT converts into a serial format to apply via the boundary-scan path. Patterns for component test may be available from an in-circuit test library or a design pattern library, or they may have to be generated manually. Cluster test patterns are usually generated manually, often with the help of a logic simulator, such as Teradyne's LASAR test simulation software.

VCCT includes the following capabilities:

- Automatic analysis of inputs and outputs of the component-under-test, plus automatic selection of the stimulus and measurement points for virtual component testing
- Powerful cluster definition language that allows a test developer to quickly identify cluster inputs and outputs which VCCT uses to select stimulus and measurement points for test
- Synchronous application of serial test patterns through the boundary-scan cells and parallel test patterns through the ATE channels

Access Analyzer (AA) Automates Pre-Layout Testability Analysis

AA tools are typically used after schematic capture and before CAD layout for assemblies that have a mix of scan and non-scan devices. AA generates two reports to help design and test engineers make the most effective use of physical and virtual access to the assembly-under-test:

- The Virtual Interconnect Test report, identifying all the pure scan nets and scan control nets (TDI/TDO interconnects) that can be fully tested by VIT and TAPIT techniques-and where physical test points can be safely eliminated.
- The Virtual Component Test report, identifying the nets where adding physical access would permit VCCT testing of non-scan devices. For in-circuit test, these nets can be accessed by a bed-of-nails probe. For edge connector test, nets can be routed to an edge connector or to a test connector for access by the ATE.

Test Access Port Integrity Testing (TAPIT) is Part of Every Test Module

Pattern generation software for pin level TAP testing is included with every VICTORY test module. TAPIT is the first VICTORY test in any assembly test sequence, executed immediately after verifying fixture contact and turning the power on.

TAPIT software performs the following tests:

- Verification of the interconnections of the four control pins in the TAP circuitry of every boundary-scan device on the assembly-under-test (five pins, if the optional Test Reset input pin is used).
- Verification that test data shifts correctly through all TAPs in the scan chain.
- Verification that the correct device is mounted in the expected location for any scan device equipped with the IDCODE instruction.

Boundary-Scan Intelligent Diagnostics (BSID) Quickly Isolates Faults

BSID installed on your test system generates high-resolution diagnostics for the following failure categories:

- TAP circuitry and chain failures detected by TAPIT
- Device failures detected by BICT
- Net failures detected by VIT
- Device or cluster failures detected by VCCT

When a boundary-scan test fails, BSID uses the failure data generated by a VICTORY module and the digital test results generated by a tester to isolate the failing devices and the networks involved. To generate diagnostics for a virtual cluster test, BSID can use fault dictionary techniques if a fault dictionary database is supplied.

BSID quickly isolates common faults such as shorts, opens, and

stuck-at pins, as well as difficult-to-detect strong driver shorts and bus faults. BSID can be run on off-line repair stations and in a wide variety of test environments (see "Supported test platforms" below).

VICTORY's Full Compliance with Current and Emerging Standards

- Accepts netlist databases from Mentor Graphics, Cadence, and Viewlogic, as well as standard EDIF data-bases, via VICTORYNet™ translation software
- Supports the Boundary-Scan Description Language (BSDL) as defined by IEEE Std 1149.1b-1994
- Test patterns are transportable to a variety of design and test environments using standard Serial Vector Format (SVF) for input and output

VICTORY Development Environments

- PC/Intel-based Windows NT® (4.0 or later), Windows® 95/98/2000/XP and Sun Solaris

Supported Test Platforms

- AccuLogic ScanMaster™
- ASSET/InterTech ASSET™
- Integrated Measurement Systems ATS test systems Intellitech Eclipse™
- Teradyne L-Series
- All Teradyne M9 Series digital instruments Teradyne Spectrum 8800-Series
- Teradyne Spectrum 9000-Series
- Teradyne Spectrum 9100-Series
- Teradyne Z1800VP-Series
- Teradyne TestStation SE
- VICTORY tests and diagnostics can be transported to any ATE platform that supports Serial Vector Format



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